Glitch free NAND based Digitally Controlled Delay Line for Spread Spectrum Clock Generator

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Abstract

NAND based digitally controlled delay-lines (DCDL) are used in wide range of applications. The existing NAND-based (DCDL) is having a glitching problem, which limit their use in many applications. This paper introduces glitch-free NAND-based DCDL which overcome the limitation of existing NANAD based DCDL. This NAND-based DCDL maintains the same resolution and minimum delay of previously proposed NAND-based DCDL. In this paper this proposed DCDL is used to realize an All-digital spread-spectrum clock generator (SSCG). The use of proposed DCDL in this circuit allows to reduce the peak-to-peak absolute output jitter of more than the 40% with respect to a SSCG using three-state inverter based DCDLs.

Keywords: *Digitally controlled delay-lines (DCDL), All-digital delay-locked loop (ADDLL), and all-digital phase-locked loop (ADPLL), spread-spectrum clock generator (SSCG).*

1. Introduction

In deep-sub micrometer CMOS processes, the time-domain resolution of a digital signal is higher than voltage resolution of analog signals .It leads towards a new circuit design in which the analog signal processing is expected to be progressively substituted by the processing of times in the digital domain. Digitally controlled delay lines (DCDL) should play the role of digital-to-analog converters in traditional, analog-intensive, circuits.

Nowadays, DCDLs are a key block in a number of applications, like all-digital PLL (ADPLL) , all-digital DLL (ADDLL), all-digital spread-spectrum clock generators (SSCGs) and ultra-wide band (UWB) receivers . The Digitally Controlled Delay Line (DCDL) is a digital circuit whose delay is controlled by a digital control word. It is having of N

identical sub-circuits, each providing 1/N of the total delay. Glitching is a common design problem in systems using DCDLs. In the most common applications, DCDLs are used to process clock signals , therefore a glitch –free operation is required. A necessary condition to avoid glitching is designing a DCDL which have no –glitch in presence of a delay control-code switching. In this paper we are going to discuss about glitch frre NAND based DCDL and its implementation on SSCG. The rest of this paper is organized in the following manner: Section II Previously Proposed NAND-Based DCDL. Section III Proposed NAND-Based DCDL. Section IV. Application to All-Digital SSCG. Section VI. SSCG Architecture.
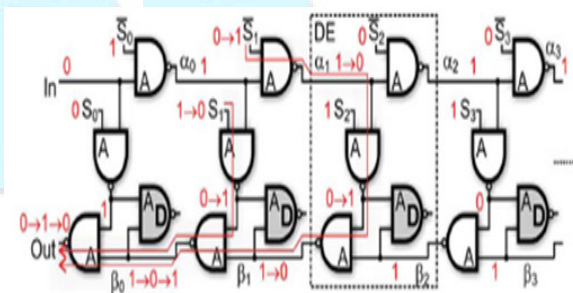
2. Previously proposed NAND -Based DCDL

Figure1: Glitching problem of NAND-based DCDL, glitching when the delay control-code increases by one

Fig. 1 shows the NAND –based DCDL. The circuit is composed by a series of equal delay –elements (DE), each composed by four NAND gates . In the figure "A" denotes the fast input of each

NAND gate. Gates marked with "D" are dummy cells added for load balancing. The delay of the circuit is controlled through control-bits Si , which encode the delay control-code c with a thermometric code $S_i=0$: for i<c, and $S_i=1$ for i>=c . By using this encoding, each DE in Fig. 1 can be either in pass-state ($S_i=0$) or in turn-state ($S_i=1$). In Fig. 1(a) all NAND gates present the same load and, therefore, in a first order approximation, present the same delay. This consideration allows to write the delay ∂ , from *In* to *Out*, as follows:

$$\partial = 2t_{NAND} + 2t_{NAND} \cdot C \qquad (1)$$

Where $t_{NAND} = (t_{NAND\ LH} + t_{NAND\ HL})/2$

while t_{NANDlh} and $t_{NAND\ HL}$ represent the delay of each NAND gate for a low-to-high and high-to-low output commutation, respectively.Equations (1) suggests that $t_{min}=2t_{NAND}$ and $t_R=2t_{NAND}$.

To avoid DCDL output glitching, the switching of delay control-bits is synchronized with the switching of *In* input signal. Glitching is avoided if the control- bits arrival time is lower than the arrival time of the input signal of the first DE which switches from or to the turn-state. Let us name S=[S0,S1,….] the vector of the control-bits of the DCDL. In Fig. 1 it is assumed that In =0 and that the control-code c of the DCDL is switched from 1 (S=[0,1,1,1…]) to 2 S=[0,0,1,1,….]) .The switching of S_1 and $S_{1\ bar}$ results in two different paths that generate an output glitch. It can be easily verified that the same glitching behavior exists when input *In* is 1.
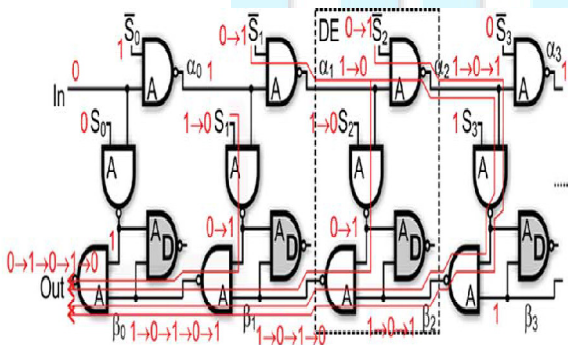
Fig.2 shows that the structure exhibits a more severe glitching problem when the delay control-code is increased by more than 1. The Fig. 2 shows the case in which control-code of the DCDL is switched from 1 (S=[0,1,1,1,….]) to 3 (S=[0,0,0,1,…]). The analysis of the figure, in this case, reveals that, four paths propagate within the DCDL structure and may create a multiple-glitch at the delay-line output.

The glitching problem of NAND-based DCDL grows up because, for a control-code equal to c, all αi and βi signals in figure 1 and 2 with i≥c, are at stuck- at 1, while for i<c the logic state of αi and βi signals depends on the input In. When the control-code is increased, the logic state of the output becomes dependant on a portion of the DCDL for which αi and βi switch from 1 to a logic state dependant on *In*. This switching may determine output glitches. This consideration also demonstrates that no glitching can occur when the control-code is decreased.
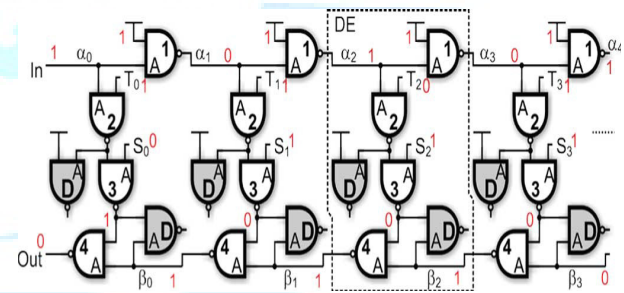
3. Proposed NAND-Based DCDL

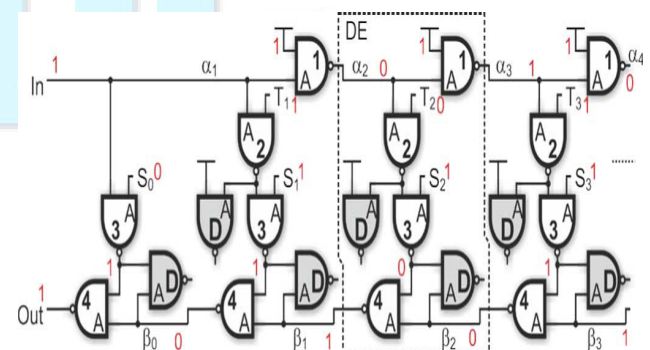Figure3 Proposed glitch-free NAND-based DCDL (inverting topology).

Figure 4 Proposed glitch-free NAND-based DCDL (non-inverting topology).

Figure2 Glitching problem of NAND-based DCDL, glitching when the delay control-code increases by Two

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The structure of proposed DCDL is shown in Fig. 3 and 4. In this Figure , "A" denotes the fast input of each NAND gate. Gates marked with "D", represents dummy cells added for load balancing. Two sets of control-bits, S_i and T_i, control the DCDL. The S_i bits encode the control-code c by using a thermometric code S_i =0: for i<c and S_i =1 for i ≥c . The bits T_i encode c again by using a one-cold code: T_{c+1}=0, T_i =1 for i≠c+1.The Fig. 8 shows the state of all signals in the case In=1,c=1. According to the chosen control-bits encoding, each delay-element (DE) can be in one of three possible states.

Table1
Logic-States of Each De in Proposed DCDLS

S_i	T_i	Delay Element State
0	1	Pass
1	1	Turn
1	0	Post-Turn

The DEs with i<c are in pass-state (S_i=0 ,T_i=1). In this state the NAND "3" output is equal to 1 and the NAND "4" allows the signal propagation in the lower NAND gates chain. The DE with i=c is in turn-state (S_i=T_i=1). In this state the upper input of the DE is passed to the output of NAND "3" . The next DE (i=c+1) is in post-turn-state (S_i=1 ,T_i=0) . In this DE, the output of the NAND "4" is stuck-at 1, by allowing the propagation, in the previous DE (which is in turn-state), of the output of NAND "3" through NAND "4". All remaining DEs (for i>c+1) are again in turn-state (S_i=T_i=1). The three possible DE states of proposed DCDL and the corresponding S_i and T_i values are summarized in Table I.

The circuit of Fig. 3 is an inverting DCDL. In this circuit the first DE is never in post-turn state, therefore to is always 1. The Fig 4 shows a non-inverting DCDL by modifying only the first DE. In this circuit the NAND gates "1" and "2" of the first DE have been deleted, together with signal T_o . The signal α_1 of the second DE is now equal to *In*, therefore the whole behavior of the DCDL is non-

inverting. This topology maintains the same t_R of previous solution.

4. Application to an All-Digital Spread Spectrum Clock Generator

To verify the usefulness of proposed solutions in a real application, the All-digital spread-spectrum clock generator (SSCG) has been redesigned by using proposed DCDL**.** Spread spectrum clocking is an effective solution to reduce the electromagnetic interference produced by digital chips, using a clock signal with a frequency that is intentionally swept(frequency modulated) within a certain frequency range, with a predefined modulation profile. There duction of the electromagnetic interference produced by digital chips has become nowadays an important design issue, due to the widespread use of digital processing techniques in consumer applications and due to the steadily increase of their operating frequency. The clocks employed in digital chips, in fact, radiate electromagnetic noise over a wide frequency band, which may interfere with other electronic equipments in the neighborhood. Spread spectrum clocking (SSC), also known as "clock dithering", is an established, cost effective, technique to reduce the EMI level. This method generates a clock signal with a frequency that is intentionally swept (frequency modulated) within a certain frequency range, with a predefined modulation profile. SSC does not actually reduce the total power of the harmonic noise but, instead, it spreads the energy of each clock harmonic evenly over a dedicated bandwidth. In this way the peak power level at each clock harmonic is reduced as much as 10–20 dB, depending on the modulation depth and the modulation profile.

A spread spectrum clock generator (SSCG) is commonly implemented with a phase-locked loop (PLL), with an appropriate frequency-modulated output. This approach use many analog blocks, which require major redesign when the technology scales down. Moreover, analog techniques do not fully exploit the speed and power improvements of CMOS processes. Finally, the bandwidth of PLL based techniques is usually limited and does not easily allow the generation of clocks with a large modulation frequency.

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5. SSCG Architecture

The top-level block diagram of the all-digital spread spectrum clock generator is shown in Fig 12. The system has an input clock signal (CLK) having a constant period $T_{CK}=1/f_{CK}$ and generates an output clock waveform , whose instantaneous period is given by

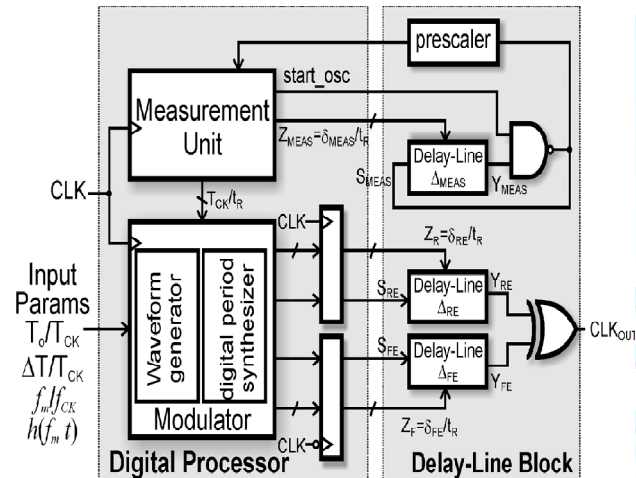$$T_{OUT}(t)=T_O +\Delta T \cdot h(f_m t) \qquad (2)$$

Figure 5 Architecture of spread spectrum clock generator.

Where T_O is the nominal output period ,ΔT is the modulation amplitude, f_m is the modulation frequency and the function $h(f_m t)$ represents the modulation profile. The function is user defined and is given by

$$0\leq h(f_m t) \leq 1 \qquad (3)$$

The instantaneous frequency of the output waveform, for an ideal down spreading modulation, is given by

$$f_{ideal}(t) = f_o - \Delta f \cdot h(f_m t) \qquad (4)$$

The SSCG in Fig. 5 is generally composed of a digital processor and a delay-line block, including two digitally controlled delay-lines (DCDLs), named Δ_{RE} and Δ_{FE} . A third replica DCDLΔ_{MEAS} , closed in a ring-oscillator topology, drives a measurement unit and is employed to compensate process, voltage, and temperature (PVT) variations. Each DCDL is driven by an input S signal and produces an output signal Y . The delay between Y and S is controlled through a digital input Z. The

digital processor receives as inputs: the period of output signal normalized to the clock period.

The digital processor receives as inputs: the period of output signal normalized to the clock period (T_O/T_{CK}) , the normalized modulation frequencyf_m/f_{CK} , the normalized modulation amplitude$\Delta T/T_{CK}$ and also the user defined modulation profile h(f_mt).We are using the input clock signalwhich has 50% duty-cycle and the SSCG is able to generate a clock signal with a frequency$f_o\leq f_{CK}$ .The output waveform signal is generated in the delay-line block. The delay-line Δ_{RE} is driven on the rising edge of the input clock and can generate an output edge in a timing window of length $T_{CK}/2$ starting from the input clock rising edge. The delay-lineΔ_{FE} can generate an output clock edge ina timing window of length $T_{CK}/2$ starting from the falling edge of the input clock signal. The XOR gate merges the two wave forms produced by the two delay lines and generates the output signal CLK$_{OUT}$. In this way the modulator is able to position the output clock edges anywhere in the time axis.
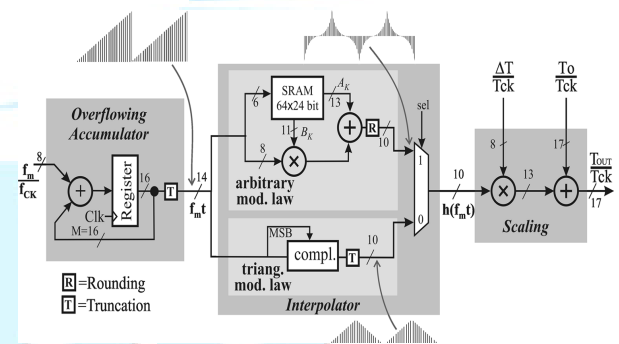
A.Modulator

1) Waveform Generator:

Fig. 6.Architecture of the waveform generator.

Fig. 6 shows the architecture of the waveform generator. It is used to compute the desired instantaneous period of the output waveform, normalized to the clock period: T_{OUT}/T_{CK}.

An M-bit overflowing accumulator is used to generate a saw tooth waveform with a frequency f_m. The modulation frequency is set with a precision of $f_{CK}/2^M$by using the control word f_m/f_{CK} . In this design M=16.The output of the overflowing

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accumulator corresponds to the argument $f_m t$ of the function h, and is truncated to 14 bits to simplify the interpolator implementation. From a practical point of view, there is no use to have a modulation frequency much larger than the maximum Resolution Bandwidth (RBW-1 MHz) considered in EMI standards. So the number of input bits used for f_m/f_{CK} is limited to 8.

The interpolator in Fig. 6 is able to generate an arbitrary waveform $h(f_m t)$.It is to be noted that interpolator can be largely simplified if only triangular modulation profile is required. In this case,

in fact, the SRAM, the multiplier and the adder can be eliminated from the circuit and replaced by a 1's complementer.

2.Digital Period Synthesizer: The digital period synthesizer generates the input signals for the two delay lines Δ_{RE} and Δ_{FE}. It is obtained with the help of a finite state machine (FSM). The outputs of the FSM (W_F and W_R) drive the two delay lines Δ_{RE} and Δ_{FE} through a scaling block.
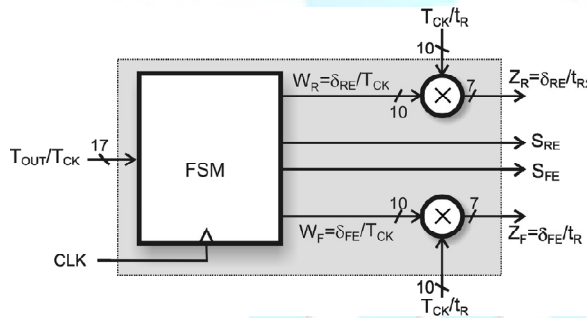

Fig. 7.Architecture of the digital period synthesizer.

B. Measurement Unit

The actual resolution of the DCDLs (t_R) depends on process, voltage, and temperature. In order to compensate PVT variations, the measurement unit continuously measures the ratio T_{CK}/t_R and sends the value of this parameter to the modulator block.
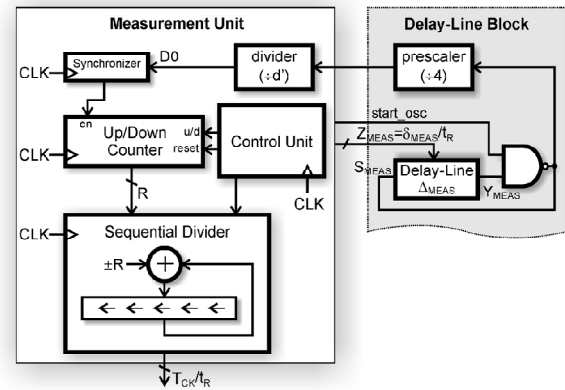

Fig. 8. Measurement unit and its connection with delay-line block.

The measurement unit is shown in Fig. 8.The DCDL Δ_{MEAS} is a replica of the DCDLs Δ_{RE} and Δ_{FE} employed to generate the output waveform. When the Signal *start_osc*is high, Δ_{MEAS} becomes part of a ring oscillator including also the NAND gate. The oscillation period can be written as

$$T_{OSC}= 2(t_{min} +Z_{MEAS} .t_R +t_{NAND}) \qquad (5)$$

where t_{min} is the minimum delay through Δ_{MEAS} and $t_{NAND}$is the delay of the NAND gate. Delay element is explained in section III.
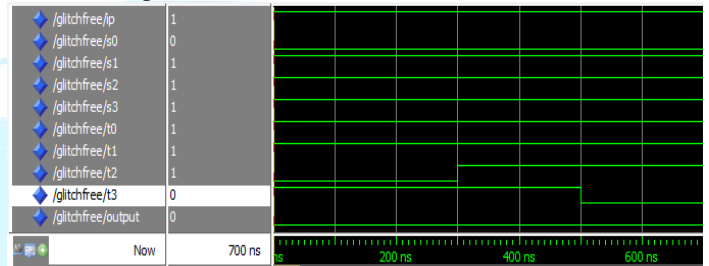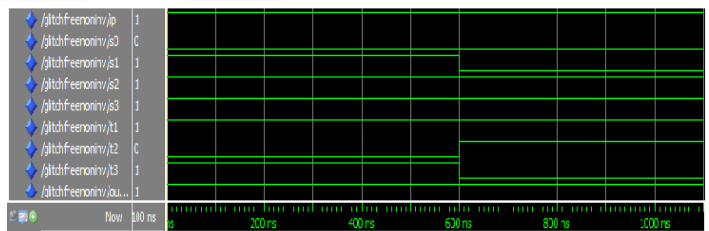

Figure9 Simulation result-Inverting topology

Figure10 Simulation result-Non-Inverting topology

Figure 9 and 10 shows the simulation results of DCDLs, when the control word is switching from 1 to 2,.In DCDLs using inverting topology, we will get get an inverted output.S0,S1,S2,S3,t0,t1.t2 and t3 are the control inputs. In non-inverting topology, we will get a non-inverting output. This DCDL is not producing any glitch during switching of the control words. Its an advantage compared with existing

6. Conclusion

A glitch free NAND-based DCDL avoids the glitching problem of previous circuit .It also provides the timing constraints that need to be imposed on the DCDL control-bits in order to guarantee a glitch-free operation. This DCDL is used to realize an all-digital SSCG. The use of proposed DCDL in this circuit allowed to reduce the peak-to-peak absolute output jitter of more than the 40% with respect to an SSCG using other DCDLs.

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